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B. E. (Sixth Semester) Examination, ~~2020~~
APR-MAY 2022
(New Scheme)

(Et & T Branch)

VLSI DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) in each question is compulsory which is of 2 marks. Attempt any two parts from the rest three, each is of 7 marks.*

Unit-I

1. (a) What is Moore's Law?

   (b) Explain VLSI design flow using flow chart?

(c) Design Nand gate using CMOS logic?

(d) Explain the static and dynamic power dissipation in CMOS inverter.

Unit-II

2. (a) Define enhancement mode in nmos transistor.

(b) Draw and explain n-well process for CMOS Fabrication.

(c) Prepare a stick diagram and schematic for 2 input CMOS NOR Gate.

(d) What is Euler Graph? Discuss with suitable example.

Unit-III

3. (a) What do you mean by layout design?

(b) Explain parity generator. Also draw its stick diagram.

(c) Sketch layout for S-R Flip-Flop.

(d) Draw and explain 4×4 NOR-ROM layout.

Unit-IV

4. (a) Define VHDL.

(b) Implement the following function using LVT for FPGA.

$$f(x_1, x_2, x_3) = x_1 \bar{x}_2 + x_1 x_3 + x_2 \bar{x}_3$$

(c) Write VLSI design style with FPGA and CPLD.

(d) Compare a VHDL source code for full adder.

Unit-V

5. (a) Define Inertial Delay model.

(b) Write a VHDL program to design JK Flip-flop.

(c) What is the difference between Melay & Moore state machine.

(d) Write a test bench for HALF ADDER.